Ordering number : EN*4907

CMOS LSI

LC75710NE, 75711NE, 75712E

Dot Matrix VFD Display Controller/Driver

Preliminary

Overview

The LC75710NE series products are dot matrix VFD controller/driver LSIs that display characters, numbers, and symbols. These LSIs generate dot matrix VFD drive signals based on serial data sent from a microprocessor, and allow display systems to be implemented easily using the built-in character generator ROM and RAM.

The LC75710NE series products are fabricated in a CMOS process and can contribute to achieving low-power operation in user applications.

Features

- 5 × 7 dot matrix VFD display controller/driver
  (Driver outputs can be connected directly to VFD devices: pull-down resistors are not required.)
- Display technique: Dynamic lighting technique
- Display digits: 1 to 16 digits (programmable)
- Display control data
  CGROM: 5 × 7 dots, 160 characters
  CGRAM: 5 × 7 dots, 8 characters
  ADRAM: 16 × 8 bits
  DCRAM: 64 × 8 bits
- Instruction functions
  Display on/off control
  Display shift
  Display blink
  Intensity adjustment (dimmer)
- Serial data input (DI, CL, and CE pins)
- Built-in reset circuit
- 64-pin flat package

Differences between the LC75710NE, LC75711NE, and LC75712E

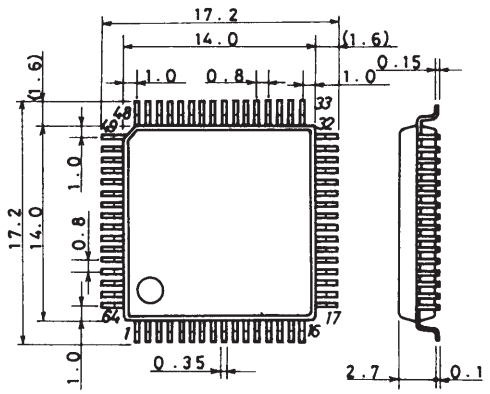
- The data in the built-in character generator ROM (CGROM) differs between these products. All other functions are identical.

Package Dimensions

unit: mm

3159-QFP64E

[LC75710NE, 75711NE, 75712E]



SANYO: QIP64E

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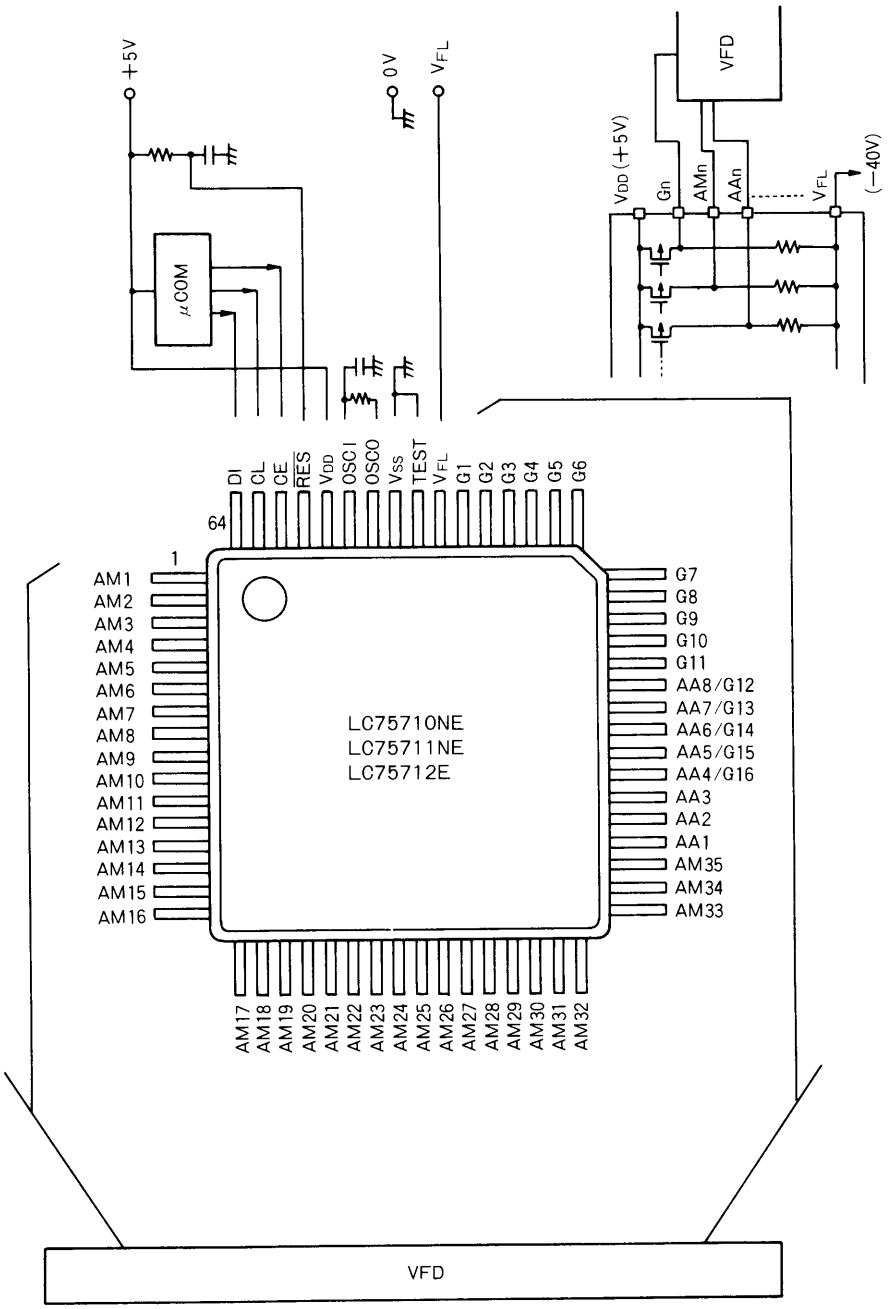
Pin Assignment and Sample Application Circuit



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +6.5	V
	V_{FL} max	V_{FL}	V_{DD} – 55 to V_{DD} + 0.3	
Input voltage	$V_{IN}1$	OSCI	–0.3 to V_{DD} + 0.3	V
	$V_{IN}2$	DI, CL, CE, $\overline{RES}$	–0.3 to +6.5	
Output current	$I_{OUT}1$	AM1 to AM35	1	mA
	$I_{OUT}2$	AA1 to AA3	10	
	$I_{OUT}3$	AA4 to AA8, G1 to G16	20	
Allowable power dissipation	Pd max	Ta ≤ 85°C, with up to 70% of the AM1 to AM35 outputs driven	400	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

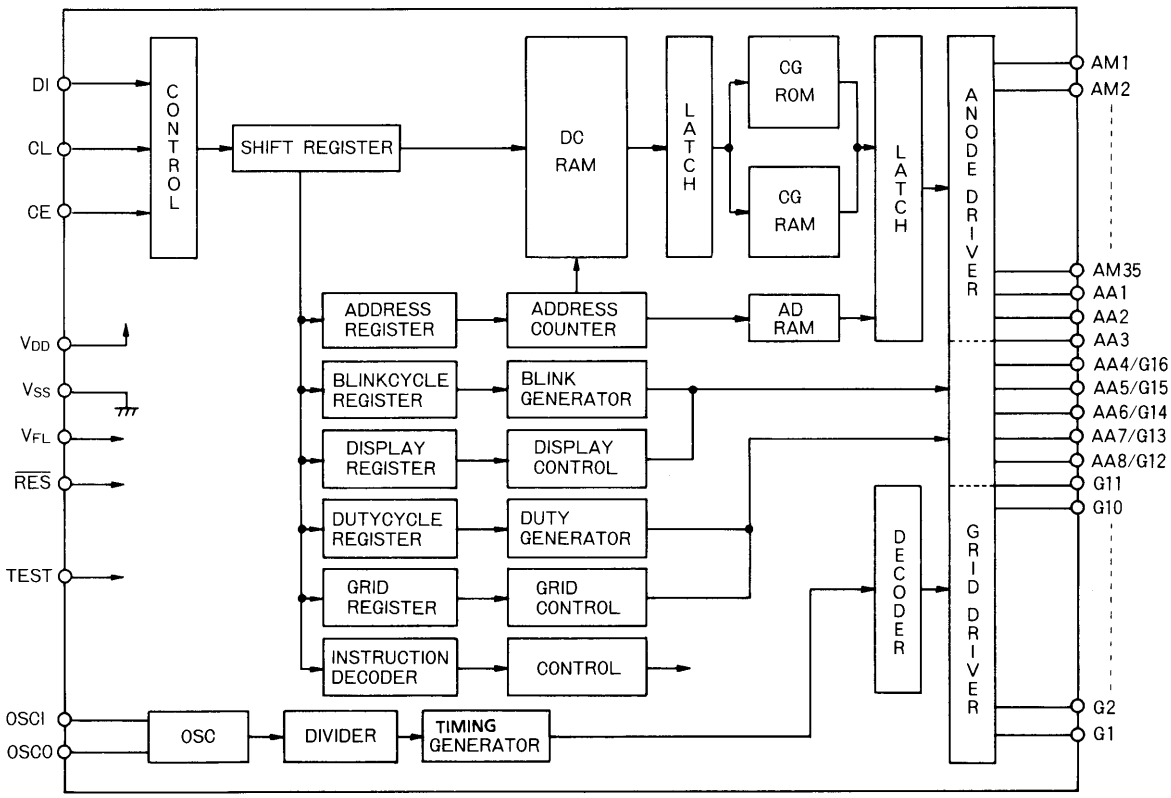
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	4.5	5.0	5.5	V
	V_{FL}	V_{FL}	V_{DD} – 50		V_{DD}	
Input high level voltage	$V_{IH}1$	DI, CL, CE	0.8 V_{DD}		5.5	V
	$V_{IH}2$	$\overline{RES}$	0.7 V_{DD}		5.5	
	$V_{IH}3$	OSCI	0.7 V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	DI, CL, CE	0		0.2 V_{DD}	V
	$V_{IL}2$	$\overline{RES}$, OSCI	0		0.3 V_{DD}	
Guaranteed oscillator range	f_{OSC}	OSCI, OSCO	1.0	2.7	3.5	MHz
Recommended external resistor	R_{OSC}	OSCI, OSCO		10		kΩ
Recommended external capacitor	C_{OSC}	OSCI, OSCO		30		pF
Minimum reset pulse width	t_{WRES}	$\overline{RES}$	1			µs
Low level clock pulse width	$t_{øL}$	CL	0.5			µs
High level clock pulse width	$t_{øH}$	CL	0.5			µs
Data setup time	t_{DS}	DI, CL	0.5			µs
Data hold time	t_{DH}	DI, CL	0.5			µs
CE wait time	t_{CP}	CE, CL	0.5			µs
CE setup time	t_{CS}	CE, CL	0.5			µs
CE hold time	t_{CH}	CE, CL	0.5			µs

Electrical Characteristics within the Allowable Operating Ranges

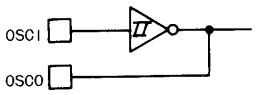
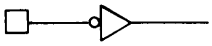
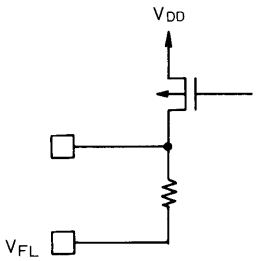
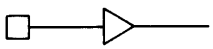
Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level current	I_{IH}	DI, CL, CE, $\overline{RES}$, OSCI: Vi = 5.5 V			5	µA
Input low level current	I_{IL}	DI, CL, CE, $\overline{RES}$, OSCI: Vi = 0 V	–5			µA
Output high level voltage	$V_{OH}1$	AM1 to AM35: I_O = 1 mA	V_{DD} – 1.0			V
	$V_{OH}2$	AA1 to AA3: I_O = 10 mA	V_{DD} – 1.0			
	$V_{OH}3$	AA4 to AA8, G1 to G16: I_O = 20 mA	V_{DD} – 2.0			
	$V_{OH}4$	OSCO: I_O = 0.5 mA	V_{DD} – 2.0		V_{DD}	
Output low level voltage	V_{OL}	OSCO: I_O = –0.5 mA	0		2.0	V
Output off voltage	V_{OFF}	AM1 to AM35, AA1 to AA8, G1 to G16: V_{FL} = V_{DD} – 50 V			V_{DD} – 49	V
Pull-down resistors	R_1	AM1 to AM35: V_{DD} – V_{FL} = 48 V	140		650	kΩ
	R_2	AA1 to AA8, G1 to G16: V_{DD} – V_{FL} = 48 V	70		325	
Oscillator frequency	f_{OSC}	R = 10 kΩ, C = 30 pF	2.16	2.7	3.24	MHz
Hysteresis voltage	V_H	DI, CL, CE	0.5			V
Supply current	I_{DD}	Outputs open, f_{OSC} = 2.7 MHz, V_{FL} = V_{DD} – 50 V			5	mA

Note: Since this IC incorporates high voltage ports it is easily damaged by static discharges. Therefore, extra care is required when handling this IC.

Block Diagram



Pin Functions

Pin	No.	Pin circuit	Function
V_{DD}	1		Logic block power supply: +5 V (typical)
V_{SS}	1		Logic block power supply: ground
V_{FL}	1		Driver block power supply
DI CL CE	1 1 1		Serial data interface DI: Transfer data CL: Synchronization clock CE: Chip enable
OSCI OSCO	1 1		External oscillator RC circuit connections
$\overline{RES}$	1		System reset input
AM1 to AM35 AA1 to AA3	38		Anode outputs Pull-down resistors are built in.
AA4/G16 AA5/G15 AA6/G14 AA7/G13 AA8/G12	5		Anode/grid outputs These pins function as grid output pins when the number of displayed digits is selected to be between 12 and 16 digits with the “Grid register load” instruction. Pull-down resistors are built in.
G1 to G11	11		Grid outputs Pull-down resistors are built in.
TEST	1		LSI testing This pin must be connected to V_{SS} during normal operation.

Block Functions

1. AC (address counter)
   AC is a counter that provides addresses for DCRAM and ADRAM.
   The address is modified automatically by internal operations to maintain the VFD display state.

2. DCRAM (data control RAM)
   DCRAM is RAM that holds the display data, which is expressed as 8-bit character codes. (These character codes are converted to 5×7 dot matrix patterns using the CGROM and CGRAM memories.) DCRAM has a capacity of 64×8 bits, and can hold the data for 64 characters. The relationship between the 6-bit DCRAM address in AC and the display position on the VFD display is described below.

   • When the DCRAM address in AC is 00_H. (16 digits displayed)

Display digit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
DCRAM address (hexadecimal)	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00

   However, the DCRAM address moves as follows when a display shift is performed by specifying MDATA.

Display digit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
DCRAM address (hexadecimal)	10	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	Right shift

Display digit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
DCRAM address (hexadecimal)	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00	3F	Left shift

   Note: The 6-bit DCRAM addresses are expressed in hexadecimal.

3. ADRAM (additional data RAM)
   ADRAM is RAM used to store ADATA display data. ADRAM has a 16×8-bit capacity and the stored display data is output directly without using CGROM and CGRAM. The relationship between the 4-bit ADRAM address in AC and the display position on the VFD display is described below.

   • When the ACRAM address in AC is 0_H. (16 digits displayed)

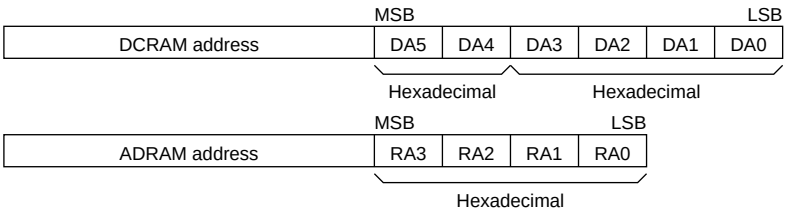
Display digit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ADRAM address (hexadecimal)	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

   However, the ADRAM address moves as follows when a display shift is performed by specifying ADATA.

Display digit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
ADRAM address (hexadecimal)	0	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	Right shift

Display digit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
ADRAM address (hexadecimal)	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	F	Left shift

   Note: DCRAM and ADRAM addresses are expressed in hexadecimal.



   Example: When the DCRAM address is $3E_H$.

DA5	DA4	DA3	DA2	DA1	DA0
1	1	1	1	1	0

4. CGROM (character generator ROM)
   CGROM is ROM that is used to generate the 160 different 5×7 dot matrix character patterns. It has a capacity of 160×35 bits. When 8-bit character codes are written to DCRAM, the CGROM character pattern corresponding to this 8-bit character code is displayed at the VFD display position corresponding to the DCRAM address in AC. Tables 3 to 5 show the correspondence between the character codes and the character patterns.

5. CGRAM (character generator RAM)
   CGRAM is RAM to which user programs can write arbitrary data. Up to eight 5×7 dot matrix character patterns can be stored in the CGRAM. CGRAM has a capacity of 8×35 bits.
   To display a character pattern stored in CGRAM, write one of the character codes shown at the left of tables 3 to 5 to DCRAM. The CGRAM character pattern will be displayed at the VFD position corresponding to the DCRAM address in AC.

Reset Function

The LC75710NE series accepts a reset when a low level is applied to the $\overline{\text{RES}}$ pin. On a reset the LC75710NE series creates a display with all VFD lamps turned off. However, note that the values in DCRAM, ADRAM, and CGRAM, as well as the values of the duty cycle register (intensity) and the grid register (number of digits) are undefined following a reset. Therefore, before turning on display with a display on/off control instruction, these values must be initialized. In particular, the following instructions must be executed when power is first applied.

- Display blink
- DCRAM data write
- ADRAM data write (if ADRAM is used)
- CGRAM data write (if CGRAM is used)
- Set AC address
- Grid register load
- Intensity adjustment (dimmer)

Initial state settings

After executing the above instructions the display must be turned on by executing a “Display on/off control” instruction.

Note that incorrect display may occur if the number of displayed digits and the intensity are not set up in advance. This can occur in cases where a display on/off control instruction is executed before the grid register load and intensity adjustment instructions are executed. To prevent this problem, always execute the following three instructions together as a single set.

- Grid register load
- Intensity adjustment (dimmer)
- Display on/off control

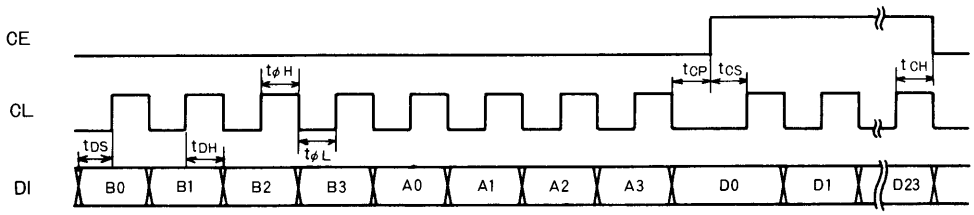
Data Input

1. Serial control data consists of an 8-bit address and a 24-bit instruction. The address is used as a chip select function when multiple ICs are connected to the same bus. The table shows the address for the LC75710NE series.

Address							
B0	B1	B2	B3	A0	A1	A2	A3
1	1	1	0	0	1	1	0

Note: Only one instruction, the “CGRAM data write” instruction, consists of 56 bits. See Table 1 for instruction code details.

2. DI, CL, CE signal timing



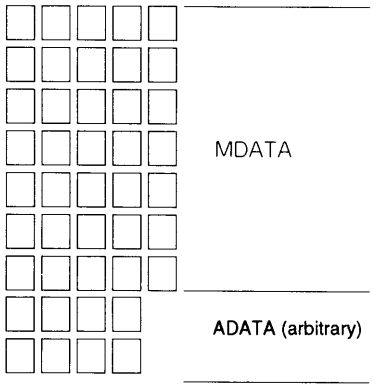
Data is acquired on the rising edge of the CL signal and latched on the falling edge of the CE signal. When the microprocessor sends multiple instructions to the LC75710NE series, it must wait long enough for the LC75710NE series to complete the execution of each instruction before sending the next instruction.

Table 1 Instruction Table

Instruction	Code																								Description	Execution time (maximum)*3
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
Display blink	1	0	1	M	A	Blink cycle data			Grid																Blinks the display. M = 1: MDATA specification, A = 1: ADATA specification*1	18 µs
Display on/off control	0	0	0	1	*	M	A	O	Grid																Turns the display on or off. O = 1: Display on, O = 0: Display off	18 µs
Display shift	0	0	1	0	*	M	A	R/L	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Shifts the display. R/L = 1: Left shift, R/L = 0: Right shift	18 µs
Grid register load	0	0	1	1	Grid number data				*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Sets the number of digits displayed according to the grid number data.	0 µs
Set AC address	0	1	0	0	ADRAM address				*	*	DCRAM address						*	*	*	*	*	*	*	*	Loads a DCRAM and ADRAM address into AC (address counter).	18 µs
Intensity adjustment (dimmer)	0	1	0	1	*	*	*	*	Duty cycle data								*	*	*	*	*	*	*	*	Adjusts the VFD intensity according to the duty cycle data.	0 µs
DCRAM data write	0	1	1	0	*	*	*	*	*	*	DCRAM address						Write data (character code)								Specifies the DCRAM (data control RAM) address and writes data.	18 µs
ADRAM data write	0	1	1	1	ADRAM address				ADATA								*	*	*	*	*	*	*	*	Specifies the ADRAM (additional data RAM) address and writes data.	18 µs
CGRAM data write	1	0	0	0	*	*	*	*	CGRAM address								Write data*2								Specifies the CGRAM (character generator RAM) address and writes data.	18 µs

*: Don't care.

Note: 1.



2. The table below shows the structure of the CGRAM data write instruction.

Code																							
D55	D54	D53	D52	D51	D50	D49	D48	D47	D46	D45	D44	D43	D42	D41	D40	D39	D38	D37	D36	D35	D34	←	→ D0
1	0	0	0	*	*	*	*	CGRAM address								*	*	*	*	*	Write data		

3. f_{OSC} = 2.7 MHz

Detailed Instruction Descriptions

1. Display blink.....<Blinks the display.>

Code																						
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	M	A	BC2	BC1	BC0	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1

M, A: Data that specifies the blinking operation

M	A	Display operating state
0	0	Neither MDATA nor ADATA blinks.
0	1	Only ADATA blinks.
1	0	Only MDATA blinks.
1	1	Both ADATA and MDATA blink.

BC0 to BC2: Blink period setting

BC2	BC1	BC0	HEX	Blink Period (s)*1 (when f_{OSC} is 2.7 MHz)
0	0	0	0	Blink operation is stopped.
0	0	1	1	0.1
0	1	0	2	0.2
0	1	1	3	0.3
1	0	0	4	0.4
1	0	1	5	0.5
1	1	0	6	0.8
1	1	1	7	1.0

G1 to G16: Blinking digit specification

Each bit Gn (where n is an integer between 1 and 16) specifies that blinking be applied to grid output pin Gn when the corresponding bit Gn is 1.

This instruction is used to specify the blinking operation. Not only can an arbitrary digit be specified, but MDATA and ADATA can also be specified. There are also seven blinking periods.

Note: 1. When the blinking period needs to be controlled precisely the display should be blinked by repeatedly turning the display on and off using the display on/off control instruction.

2. Display on/off control.....<Turns the display on or off.>

Code																						
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	M	A	O	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1

*: Don't care.

M, A: Specifies the data to be turned on or off.

M	A	Display operating state
0	0	Both MDATA and ADATA turn off.
0	1	Only ADATA turns on.
1	0	Only MDATA turns on.
1	1	Both ADATA and MDATA turn on.

O: On/off control

O	Display state
0	Off
1	On

When the display is turned off with an O value of 0, the data can be displayed immediately with an O value of 1 since the display data remains in DCRAM.

G1 to G16: Display digit specification
Each bit Gn (where n is an integer between 1 and 16) specifies that the corresponding grid output pin Gn be turned on when that bit (Gn) is 1.
This instruction is used to specify the display on/off control operation. Not only can an arbitrary digit be specified, but MDATA and ADATA can also be specified.

3. Display shift .....<Shifts the display.>

Code																						
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	*	M	A	R/L	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

*: Don't care.

M, A: Specifies the data to be shifted.

M	A	Shift operating state
0	0	Neither MDATA nor ADATA are shifted.
0	1	Only ADATA is shifted.
1	0	Only MDATA is shifted.
1	1	Both MDATA and ADATA are shifted.

R/L: Shift direction specification

R/L	Shift direction
0	Right shift
1	Left shift

4. Grid register load .....<Specifies the number of digits displayed.>

Code																						
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	GN3	GN2	GN1	GN0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

*: Don't care.

GN0 to GN3: Displayed digits specification

GN3	GN2	GN1	GN0	HEX	Digits Controlled
0	0	0	0	0	G1 to G16
0	0	0	1	1	G1
0	0	1	0	2	G1 to G2
0	0	1	1	3	G1 to G3
0	1	0	0	4	G1 to G4
0	1	0	1	5	G1 to G5
0	1	1	0	6	G1 to G6
0	1	1	1	7	G1 to G7
1	0	0	0	8	G1 to G8
1	0	0	1	9	G1 to G9
1	0	1	0	A	G1 to G10
1	0	1	1	B	G1 to G11
1	1	0	0	C	G1 to G12
1	1	0	1	D	G1 to G13
1	1	1	0	E	G1 to G14
1	1	1	1	F	G1 to G15

The AA4/G16, AA5/G15, AA6/G14, AA7/G13, and AA8/G12 anode/grid output pins function as grid output pins if between 12 and 16 digits are selected. Also, this instruction must be executed prior to turn the display on since the value of the grid register is undefined immediately after power is applied.

5. Set AC address.....<Specifies the DCRAM and ADRAM addresses for AC.>

Code																							
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	RA3	RA2	RA1	RA0	*	*	DA5	DA4	DA3	DA2	DA1	DA0	*	*	*	*	*	*	*	*

*: Don't care.

DA0 to DA5: DCRAM address
DA0.....LSB (least significant bit)
DA5.....MSB (most significant bit)

RA0 to RA3: ADRAM address
RA0.....LSB
RA3.....MSB

This instruction loads the 6-bit DA0 to DA5 DCRAM address and the 4-bit RA0 to RA3 ADRAM address into AC.

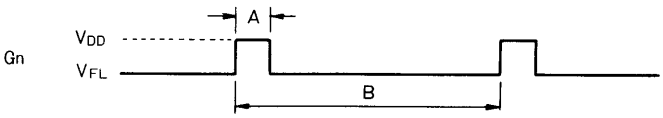
6. Intensity adjustment.....<Adjusts the VFD intensity.>

Code																							
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	*	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0	*	*	*	*	*	*	*	*

*: Don't care.

DC0 to DC7: Duty cycle data (intensity adjustment data)
DC0.....LSB
DC7.....MSB

The data in the 8 bits DC0 to DC7 sets the VFD intensity to one of 240 levels. Since the value in the duty cycle register is undefined immediately after power is applied, the display intensity is not determined at that point. Therefore, applications must execute this instruction before turning on the display. Applications can adjust the intensity using the duty cycle register and grid register. The duty cycle register value sets the pulse width (A) and the grid register value sets the period (B). See Figure 3 for the grid timing chart details.



7. DCRAM data write.....<Specifies the DCRAM address and stores data at that address.>

Code																							
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	*	*	*	*	*	*	DA5	DA4	DA3	DA2	DA1	DA0	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0

*: Don't care.

DA0 to DA5: DCRAM address
DA0.....LSB
DA5.....MSB

AC0 to AC7: DCRAM write data (character code)
AC0.....LSB
AC7.....MSB

This instruction writes the 8 bits of data AC0 to AC7 to DCRAM. This data is a character code (see Tables 3 to 5) and is converted to 5×7 dot matrix display data using CGROM and CGRAM.

8. ADRAM data write.....<Specifies the ADRAM address and stores data at that address.>

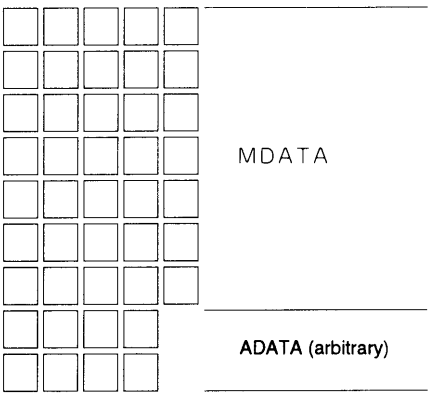
Code																							
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	RA3	RA2	RA1	RA0	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	*	*	*	*	*	*	*	*

*: Don't care.

RA0 to RA3: ADRAM address
RA0.....LSB
RA3.....MSB

AD1 to AD8: ADATA display data

There are 8 bits of additional display data, referred to as ADATA, in addition to the 5×7 dot matrix of display data (MDATA). This data is used to generate arbitrary dot patterns without using CGROM or CGRAM. The figures show the correspondence between these data types. In particular, when ADn = 1 (where n is an integer between 1 and 8), the dot AAn will be turned on.



ADATA	Corresponding output pin
AD1	AA1
AD2	AA2
AD3	AA3
AD4	AA4/G16
AD5	AA5/G15
AD6	AA6/G14
AD7	AA7/G13
AD8	AA8/G12

9. CGRAM data write .....<Specifies the CGRAM address and stores data at that address.>

Code															
D55	D54	D53	D52	D51	D50	D49	D48	D47	D46	D45	D44	D43	D42	D41	D40
1	0	0	0	*	*	*	*	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

Code															
D39	D38	D37	D36	D35	D34	D33	D32	D31	D30	D29	D28	D27	D26	D25	D24
*	*	*	*	*	CD35	CD34	CD33	CD32	CD31	CD30	CD29	CD28	CD27	CD26	CD25

Code															
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8
CD24	CD23	CD22	CD21	CD20	CD19	CD18	CD17	CD16	CD15	CD14	CD13	CD12	CD11	CD10	CD9

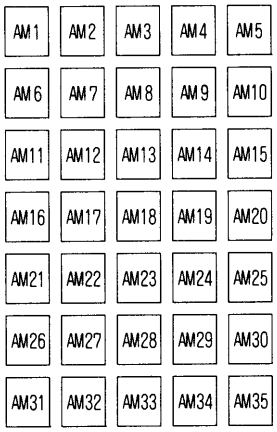
Code							
D7	D6	D5	D4	D3	D2	D1	D0
CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1

*: Don't care.

CA0 to CA7: CGRAM address
CA0 .....LSB
CA7 .....MSB

CD1 to CD35: CGRAM write data (5×7 dot matrix display data)

The bit CDn (where n is an integer between 1 and 35), corresponds to the AMn dot display data. The figure below shows the positional relationship for this display data.



Usage Notes

1. Power supply sequence
   The sequences shown below must be followed when turning the power supply on and off. (See Figure 1.)
   Power on: Logic block power supply (V_{DD}) on → Driver block power supply (V_{FL}) on → Display on (by the execution of a display on/off control instruction)
   Power off: Display off (by the execution of a display on/off control instruction) → Driver block power supply (V_{FL}) off → Logic block power supply (V_{DD}) off

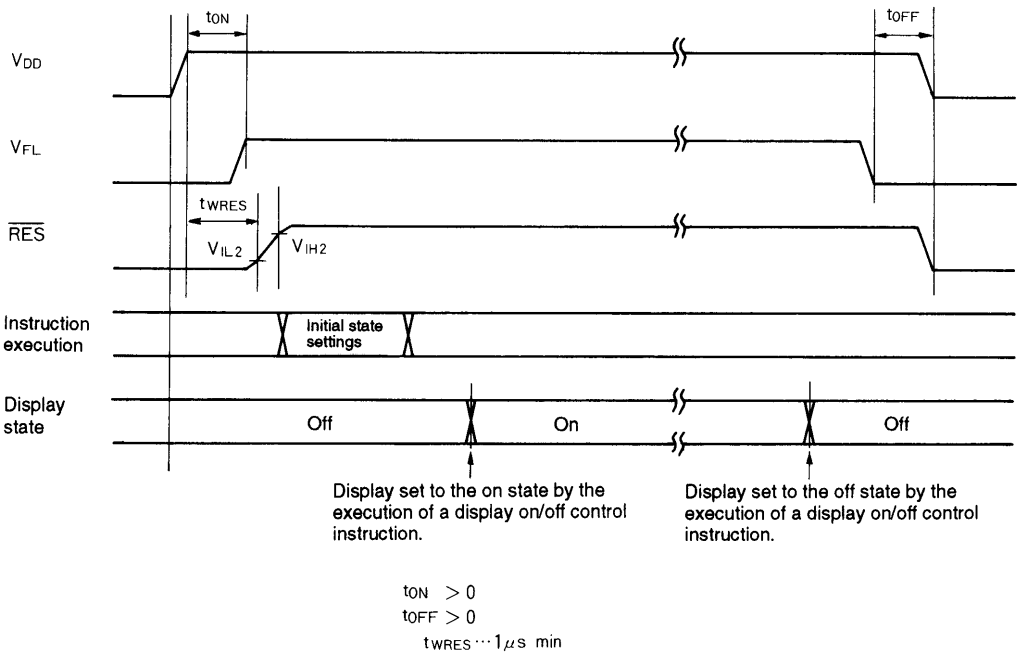


Fig. 1 Power Supply Sequence

2. Anode output pins
   The anode output pins AM1 to AM35 are used as the anode outputs that form the 5 × 7 dot matrix due to output current considerations. We recommend using the anode output pins AA1 to AA8 for other anode output functions. If the anode waveform is distorted and the VFD glows slightly (smearing) due to the VFD panel used or wiring considerations, try using a lower oscillator frequency. Refer to Figure 2 when determining the oscillator frequency.

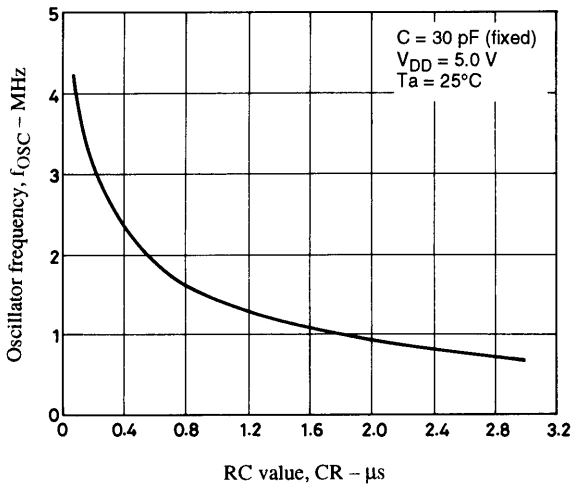


Fig. 2 Oscillator Frequency

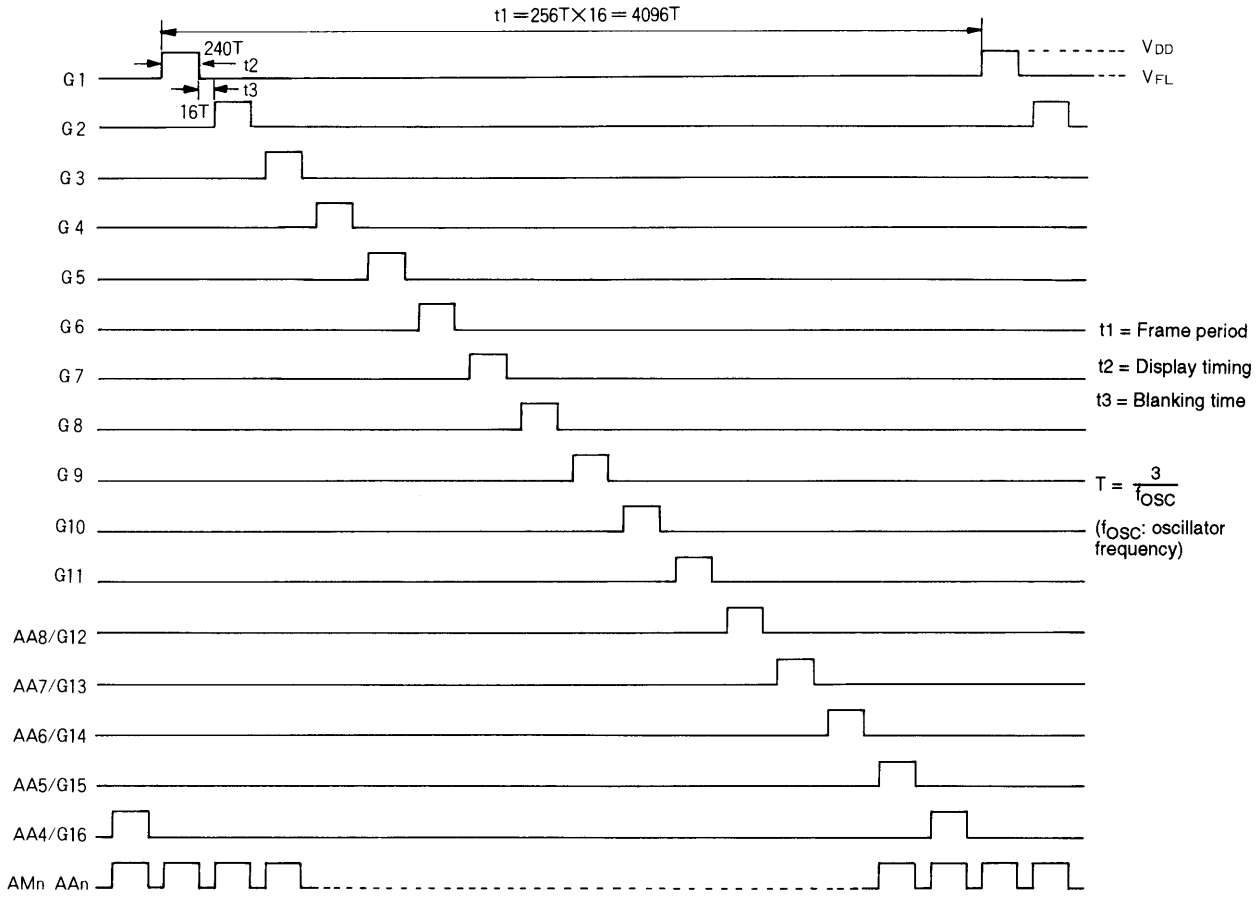


Fig. 3 Grid Timing Chart (16 display digits)

Table 2 Instruction/Display Correspondence (LC75710NE)

No.	Instruction (hexadecimal)	Display	Operation
1	Power application (Initialization with the $\overline{\text{RES}}$ pin)		Initializes the IC. The display will be in the off state.
2	DCRAM data write 6 * 0 0 2 0		Writes display data " " to DCRAM address 00H.
3	DCRAM data write 6 * 0 1 4 F		Writes display data "O" to DCRAM address 01H.
4	DCRAM data write 6 * 0 2 5 9		Writes display data "Y" to DCRAM address 02H.
5	DCRAM data write 6 * 0 3 4 E		Writes display data "N" to DCRAM address 03H.
6	DCRAM data write 6 * 0 4 4 1		Writes display data "A" to DCRAM address 04H.
7	DCRAM data write 6 * 0 5 5 3		Writes display data "S" to DCRAM address 05H.
8	DCRAM data write 6 * 0 6 2 0		Writes display data " " to DCRAM address 06H.
9	DCRAM data write 6 * 0 7 2 0		Writes display data " " to DCRAM address 07H.
10	DCRAM data write 6 * 3 D 4 9		Writes display data "I' to DCRAM address 3DH.
11	DCRAM data write 6 * 3 E 5 3		Writes display data "S" to DCRAM address 3EH.
12	DCRAM data write 6 * 3 F 4 C		Writes display data "L" to DCRAM address 3FH.
13	Grid register load 3 8 * * * *		Specifies that the display has 8 digits.
14	Intensity adjustment 5 * F F * *		Sets the VFD intensity to the maximum.
15	Display on/off control 1 5 0 0 F F	S A N Y O	Turns on the VFD for only the digits G1 to G8 in MDATA.
16	Display shift 2 5 * * * *	S A N Y O L	Shifts the display (MDATA only) to the left.
17	Display shift 2 5 * * * *	S A N Y O L S	Shifts the display (MDATA only) to the left.
18	Display shift 2 5 * * * *	A N Y O L S I	Shifts the display (MDATA only) to the left.
19	Set AC address 4 * 0 0 * *	S A N Y O	Returns the display to the original state.

* Don't care.
Note: The example above assumes the use of an 8 digit 5 × 7 dot matrix VFD, and CGRAM and ADRAM are not used.

Table 3 LC75710NE CGROM (Version for use in USA and Japan)

Upper 4 bits / Lower 4 bits	MSB 0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101
0000 LSB	CG RAM(1)		0	@	P	＼	p		ー	タ	ミ
0001	(2)	!	1	A	Q	a	q	。	ア	チ	ム
0010	(3)	”	2	B	R	b	r	「	イ	ツ	メ
0011	(4)	#	3	C	S	c	s	」	ウ	テ	モ
0100	(5)	$	4	D	T	d	t	、	エ	ト	ヤ
0101	(6)	%	5	E	U	e	u	・	オ	ナ	ユ
0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ
0111	(8)	’	7	G	W	g	w	ア	キ	ヌ	ラ
1000		(	8	H	X	h	x	イ	ク	ネ	リ
1001		)	9	I	Y	i	y	ウ	ケ	ノ	ル
1010		＊	:	J	Z	j	z	エ	コ	ハ	レ
1011		＋	;	K	〔	k	{	オ	サ	ヒ	ロ
1100		,	<	L	¥	l	|	ヤ	シ	フ	ワ
1101		―	=	M	〕	m	}	ユ	ス	ヘ	ン
1110		.	>	N	＾	n	→	ヨ	セ	ホ	゛
1111		/	?	O	_	o	←	ッ	ソ	マ	゜

Note: The character pattern (output data) is undefined if the character codes 00001000_B to 00011111_B, 10000000_B to 10011111_B, or 11100000_B to 11111111_B are written to DCRAM.

Table 4 LC75711NE CGROM (Version for use in Europe)

Upper 4 bits / Lower 4 bits	MSB 0000	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011
0000 LSB	CG RAM(1)		0	@	P	‖	p	á	â	a	O
0001	(2)	!	1	A	Q	a	q	à	ä	α	Φ
0010	(3)	”	2	B	R	b	r	é	ê	Ö	ã
0011	(4)	#	3	C	S	c	s	è	ë	Å	å
0100	(5)	$	4	D	T	d	t	í	î	Ğ	±
0101	(6)	%	5	E	U	e	u	ì	ï	ğ	İ
0110	(7)	&	6	F	V	f	v	ó	ô	ŋ	ń
0111	(8)	’	7	G	W	g	w	ò	ö	Æ	æ
1000		(	8	H	X	h	x	ú	û	π	μ
1001		)	9	I	Y	i	y	ù	ü	Œ	¿
1010		*	:	J	Z	j	z	Ñ	ñ	£	÷
1011		+	;	K	[	k	{	Ç	ç	$	ce
1100		,	<	L	\	l	|	Ş	ş	←	ϕ
1101		−	=	M	]	m	}	ß	ğ	↑	Ω
1110		.	>	N	^	n	—	¡	ı	→	Σ
1111		/	?	O	_	o	■	Ü	Ä	↓	§

Note: The character pattern (output data) is undefined if the character codes 00001000_B to 00011111_B or 11000000_B to 11111111_B are written to DCRAM.

Table 5 LC75712E CGROM (Version for use in Europe)

Upper 4 bits / Lower 4 bits	MSB 0000	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011
0000 LSB	CG RAM(1)		0	@	P	‖	p	á	Ä	Á	Ã
0001	(2)	!	1	A	Q	a	q	à	ä	À	ã
0010	(3)	”	2	B	R	b	r	é	Ë	É	Å
0011	(4)	#	3	C	S	c	s	è	ë	È	å
0100	(5)	¤	4	D	T	d	t	í	Ï	Í	Æ
0101	(6)	%	5	E	U	e	u	ì	ï	Ì	æ
0110	(7)	&	6	F	V	f	v	ó	Ö	Ó	Œ
0111	(8)	’	7	G	W	g	w	ò	ö	Ò	œ
1000		(	8	H	X	h	x	ú	Ü	Ú	Õ
1001		)	9	I	Y	i	y	ù	ü	Ù	õ
1010		✳	:	J	Z	j	z	Ñ	ñ	£	÷
1011		+	;	K	[	k	{	Ç	ç	$	°
1100		,	<	L	\	l	|	π	±	←	Φ
1101		−	=	M	]	m	}	ß	μ	↑	φ
1110		.	>	N	^	n	~	¡	¿	→	¯ ±
1111		/	?	O	_	o	■	Ü	ij	↓	§

Note: 1. The character pattern (output data) is undefined if the character codes 00001000_B to 00011111_B or 11000000_B to 11111111_B are written to DCRAM.

2. Both the LC75711NE and the LC75712E are for use in the European market. These products differ in that the LC75712E CGROM takes handling a 5×8 dot matrix into consideration. In particular, this product allows the AA1 to AA5 anode output pins to be used to form a 5×8 dot matrix artificially, with the combination of AM1 to AM35 and AA1 to AA5. Adopting this structure allows applications to provide improved display quality for European characters, especially those requiring an umlaut.